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جامعة بيرزيت
BIRZEIT UNIVERSITY

ENCS 2110
DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY

Quiz 1 – a **name & id:** Roa [illegible] Nafi , 1201959

Q1. Given the logic system is shown in Fig. 1.17
output of the system F is in"1"state in each of the **following condition**

- A ,B are in the "1" state, C in "0" state. $AB\bar{C}$
- A, B and D are in the "1" state ABD
- C is in the "1" state A, B and D are in the "0" state. $C\bar{A}\bar{B}\bar{D}$

DO NOT USE TRUTH TABLE

1. **Write the boolean full equation as canonical sum.**

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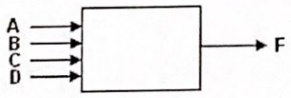

Fig. 1.17 Block diagram

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

$F = AB\bar{C} + ABD + C\bar{A}\bar{B}\bar{D}$

$= AB\bar{C}D + AB\bar{C}\bar{D} + ABCD + AB\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}$
1101 1100 1111 1101 0010

$= m_{13} + m_{12} + m_{15} + m_{13} + m_2$

$= \Sigma\, 2, 12, 13, 15$

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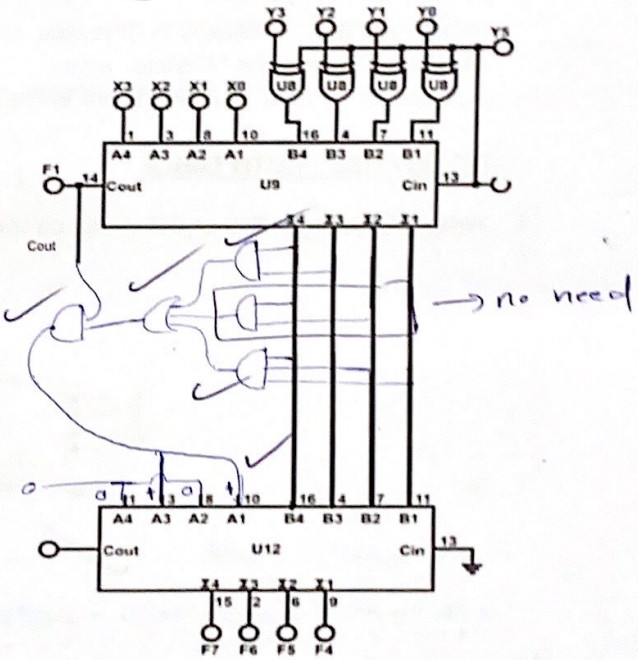
Q2. Complete the following diagram, to create a BCD adder that counts to 10 instead of 9



Q3. a circuit that converts n inputs to 2^n outputs is called :

a. Decoder b. Encoder c. Multiplexer d. Flip-Flop

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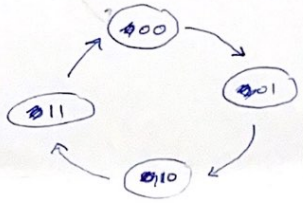
Quiz 3 **name & id:** Roa Nafi

1- Design a 2-bit **Synchronous** Counter Using J-K Flip Flops. Show all your work including truth tables, and boolean expressions used. In addition to the designed circuit diagram.

2-bit Synchronous Counter counts from 0 to 3 and return to count from 0 ;

P.S | N.S | $J_1 K_1$ | $J_0 K_0$

Q_1	Q_0	Q_1	Q_0	J_1	K_1	J_0	K_0
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1



$Q_1 Q_0$	J	K
0 0	0	X
0 1	1	X
1 0	X	1
1 1	X	0

J_1

Q_1 \ Q_0	0	1
0		1
1	X	X

$\rightarrow Q_0$

J_0

Q_1 \ Q_0	0	1
0	1	X
1	1	X

$\rightarrow \bar{Q}_0$ use don't cares

$J_0 = 1$

K_1

Q_1 \ Q_0	0	1
0	X	X
1		1

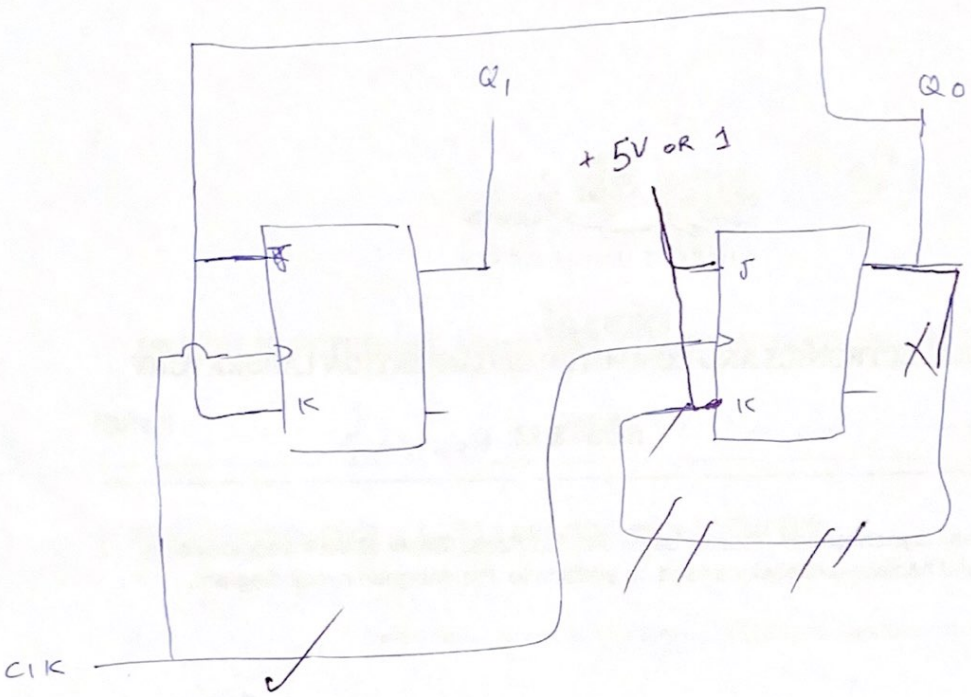
$\rightarrow Q_0$

K_0

Q_1 \ Q_0	0	1
0	X	
1	X	1

$\rightarrow Q_0$

$K_0 = 1$


Q_1
Q_0
+5V OR 1
J
K
J
K
CLK

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Quiz 5 **name & id:** Roa Nafi 1201959

1- Write a verilog code to build a **negative edge** D Flip Flop

```
module DFlipFlop ( D, Q);
 input D;
 output reg Q;
 always @ ( negedge CLK)
  begin
    Q <= D;
  end
end module
```